This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An integrated circuit fabrication process, the process comprising the steps of:

patterning a transistor gate pattern on a photoresist layer;

curing the transistor gate pattern with an electron beam;

trimming the cured transistor gate pattern; and

transferring the trimmed transistor gate pattern to a layer disposed below the ~~photoresist layer~~ trimmed pattern to form a transistor gate, wherein the transistor gate includes a width and a length, and a variation of the width along the length of the transistor gate is reduced due to the curing step.

2. (Previously Presented) The process of claim 1, wherein the photoresist layer is comprised of a photoresist material used for at least one of 248 nm lithography, 193 nm lithography, and extreme ultraviolet light (EUV) lithography.

3. (Currently Amended) The process of claim 2, wherein the photoresist layer is comprised of a photoresist material of a type ~~typically~~ used for 193 nm and 248 nm lithography and is commercially available.

4. (Original) The process of claim 1, wherein the final gate transistor width is in the range of approximately 20-60 nm.

5. (Original) The process of claim 1, wherein the curing step includes exposing the transistor gate pattern to the electron beam having a dose in the range of approximately 100-100000 $\mu C/cm^2$.

6. (Previously Presented) The process of claim 1, wherein the curing step includes exposing the transistor gate pattern to the electron beam having an accelerating voltage in the range of approximately 50-2000 Volts.

7. (Original) The process of claim 1, wherein the curing step includes changing at least one of a vertical etch rate, a horizontal etch rate, and a minimum extension erosion rate associated with the transistor gate pattern.

8. (Previously Presented) A method of forming a transistor having a gate width of less than 70 nm, the method comprising the steps of:

E-beam irradiating a gate pattern of a photoresist layer;

trimming the E-beam irradiated gate pattern of the photoresist layer; and

etching a polysilicon layer disposed below the photoresist layer in accordance with the trimmed gate pattern to form a gate of the transistor, the gate width being less than 70 nm.

9. (Previously Presented) The method of claim 8, wherein the E-beam irradiating step uses an electron beam at a dose in the range of approximately 100-100000 $\mu C/cm^2$.

10. (Previously Presented) The method of claim 9, wherein the electron beam is provided at an accelerating voltage in the range of approximately 50-2000 Volts.

11. (Previously Presented) The method of claim 9, wherein a uniformity of the gate width is 4 to 6 nm over a 3 nm segment.

12. (Previously Presented) The method of claim 9, wherein the photoresist layer is comprised of a material selected from a group consisting of an acrylate-based polymer, alicyclic-based polymer, phenolic-based polymer, and a polystyrene-based polymer.

13. (Previously Presented) The method of claim 9, wherein the E-beam irradiation step includes affecting at least one of a vertical etch rate, a horizontal etch rate, and a minimum extension erosion rate associated with the gate pattern of the photoresist layer.

14. (Previously Presented) The method of claim 9, wherein the E-beam radiation step achieves an enhancement interim rate for a commercially available resists using lithography processes with either 248 nm and 193 nm wavelength of light.

15-20 (Cancelled)

21. (Previously Presented) A method of producing an integrated circuit comprising:

providing a photoresist material over a substrate;

irradiating a portion of the photoresist material with an electron beam to form a gate pattern;

trimming the gate pattern; and

etching the substrate in accordance with the gate pattern to form a gate, the gate having a width of less than 70 nm.

22. (Previously Presented) The method of claim 21, wherein the electron beam is provided at an accelerating voltage in the range of approximately 0.5-50 Kv.

23. (Previously Presented) The method of claim 21, wherein the photoresist layer is comprised of a material selected from a group consisting of an acrylate-based polymer, an alicyclic-based polymer, a phenolic-based polymer, and a polystyrene-based polymer.

24. (Previously Presented) The method of claim 21, wherein the step of irradiating a portion of the photoresist material includes affecting at least one of a vertical etch rate, a horizontal etch rate, and a minimum extension erosion rate associated with the gate pattern of the photoresist layer.

25. (Previously Presented) The method of claim 21, wherein the step of irradiating a portion of the photoresist material achieves an enhancement interim rate for a photoresist material using lithography processes with either 248 nm and 193 nm wavelength of light.

26. (Previously Presented) The method of claim 21, wherein the photoresist material may be used with at least one of 248 nm lithography, 193 nm lithography, and extreme ultraviolet (EUV) lithography.